ABSTRACT OF THE INVENTION

The packet-buffering system and method of the present invention enables communication devices incorporating a full-mesh architecture to achieve bandwidth aggregation levels ordinarily associated with partial-mesh architectures. The packet-buffering invention uses a hierarchical memory structure having first and second packet-buffers to buffer packets between the input and output ports of the communication device. The received packets are organized by output port and priority level in the first packet buffer, which operates at the aggregate network rate of the communication device. The packets are then funneled to second packet buffers, having corresponding priority and output port assignments, at less than the aggregate network rate and which exhibit buffer depths that exceed that of the first packet buffer. The resulting hierarchical output-queued, packet-buffering system enables a communication system that exhibits a high degree of differentiated services with bandwidth guarantees and at high aggregation levels without experiencing head-of-line blocking.

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